REMARKS/ARGUMENTS

Claim Rejections – 35 USC 102

Claims 1-3, 6-10, 12-16, 19-23, and 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Ochiai (USPN 6862688B2).

5   Response:

Claims 1 and 14

The applicant asserts that Ochiai does not anticipate applicant's claim 1, as Ochiai fails to teach the claimed features "each higher-level subroutine used for <u>calling</u> at least <u>a lower-level subroutine</u> to control the hardware circuit to execute operations

10   corresponding to <u>the lower-level subroutine called by the higher-level subroutine</u>", "each <u>the lower-level subroutine will record operation results</u>, which come from the hardware circuit executing corresponding operations, <u>in an error code</u>", "an error-handling subroutine for <u>calling the recovery subroutines according to the error code</u>," and "after the processor executes the higher-level subroutine, <u>executing the</u>

15   <u>error-handling subroutine</u> to allow the processor to control the hardware circuit to execute recovery operations <u>according to the operation results corresponding to the lower-level subroutine called by the higher-level subroutine</u>" as recited in applicant's claim 1. (*emphasis added*) In other words, the applicant asserts that the claimed hierarchical software structure having subroutine calls included therein is not

20   anticipated by teaching of Ochiai.

Upon thorough review of teachings of Ochiai, the applicant respectfully points out that the key feature of Ochiai's fault handling system and method is to adaptively change the type of fault information recording processing and/or fault recovery processing optimum according to the operation mode information of the information

25   processing system and the fault class information of the detected fault (col. 5, lines 25-36; col. 8, lines 57-67; col. 11, lines 12-21; col. 12, lines 37-49; col. 14, lines 47-59; col. 17, lines 47-59; col. 19, lines 50-64; col. 21, line 62-col. 22, line 7). However, Ochiai's disclosure fails to teach or suggest the implementation of a hierarchical software structure, explicitly or implicitly. More specifically, as one can

see from drawing figures 2, 4, 6, 7, 9, 11, 13, and 15 of Ochiai's disclosure, these exemplary fault handling systems shown therein employ the same fault detecting section (reference numeral 100); in addition, Ochiai's disclosure further explicitly states:

5   *"A reference numeral 100 denotes a fault detecting section for detecting a fault in the information processing system and for judging and identifying fault information 101 and fault class information 102 indicating the degree of seriousness of the fault (col. 5, lines 43-47)"*.

Note is therefore respectfully made by the applicant that Ochiai does teach the
10   fault information and recording the fault information; however, Ochiai fails to teach or suggest that the fault information is recorded when executes a lower-level subroutine called by a higher-level subroutine, and the fault recovery processing is applied according to the recorded fault information. Briefly summarized, as Ochiai's fault handling system and method include no hierarchical software structure involved
15   therein, Ochiai's disclosure is therefore silent on executing an error-handling subroutine to execute recovery operations according to the fault information corresponding to the lower-level subroutine called by the higher-level subroutine.

Compared with teachings of Ochiai, applicant's claim 1, however, claims that each higher-level subroutine <u>calls</u> at least a lower-level subroutine to control the
20   hardware circuit to execute operations corresponding to the lower-level subroutine <u>called</u> by the higher-level subroutine, <u>the operation result</u> of the lower-level subroutine <u>called</u> by the higher-level subroutine is <u>stored in an error code</u>, and an error-handling subroutine <u>calls</u> recovery subroutines <u>according to the error code</u>, each recovery subroutine corresponding to a recovery operation. (*emphasis added*)

25   In conclusion, as none of the lower-level subroutines, higher-level subroutines and limitations mentioned above recited in applicant's claim 1 is disclosed by Ochiai, the claimed method having these particular subroutines involved therein is not anticipated by Ochiai. In addition, for example, the claimed limitation "after the processor executes the <u>higher-level subroutine</u>, executing the <u>error-handling</u>

<u>subroutine</u> to allow the processor to control the hardware circuit to execute recovery operations according to the operation results corresponding to the <u>lower-level subroutine called by the higher-level subroutine</u>" is would never be anticipated by the cited prior art. (*emphasis added*) Withdrawal of the rejection and reconsideration of independent claim 1 are respectfully requested.

Furthermore, in view of above arguments of claim 1, the applicant asserts that claim 14, having similar limitations recited in claim 1, should be found allowable over the cited Ochiai reference. Withdrawal of the rejection and reconsideration of independent claim 14 are respectfully requested as well.

<u>Claims 2-3, 6-10, 12-13, 15-16, 19-23, and 25-28</u>

Claims 2-3, 6-10, 12-13, 15-16, 19-23, and 25-28 are dependent upon claims 1 and 14 respectively, and include further limitations added to respective claims 1 and 14. As claims 1 and 14 contain claimed features patentable over the cited prior art, claims 2-3, 6-10, 12-13, 15-16, 19-23, and 25-28 therefore should be found allowable. Withdrawal of the rejections and reconsideration of claims 2-3, 6-10, 12-13, 15-16, 19-23, and 25-28 are respectfully requested.

Claim Rejections – 35 USC 103

Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Sim et al. (USPN 6785212B1).

Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Okada et al. (USPN 6530034B1).
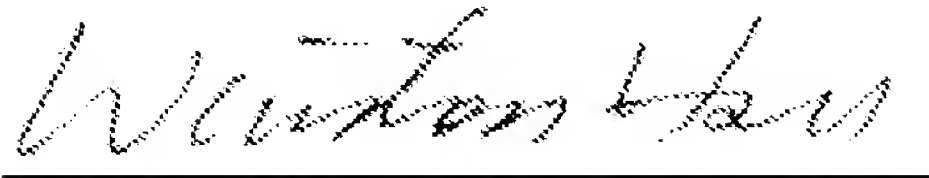
Response:

Claims 4-5 and 17-18 are dependent upon claims 1 and 14 respectively, and include further limitations added to respective claims 1 and 14. As claims 1 and 14 contain claimed features patentable over the cited prior art, claims 4-5 and 17-18 therefore should be found allowable. Withdrawal of the rejections and reconsideration of claims 4-5 and 17-18 are respectfully requested.

Conclusion

Based on the above remarks/arguments, the applicant respectfully submits that all of the rejections set forth in the Office Action dated 03/18/2008 have been
5 overcome and the pending claims are now in condition for allowance. The applicant therefore respectfully requests that a timely Notice of Allowance be issued in this case. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact the undersigned applicant's representative at the number indicated below.
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Sincerely yours,

Date: 06.18.2008

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